Power-decoupling of a Multi-port Isolated Converter for an Electrolytic-capacitorless Multi-level Inverter

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Abstract — This paper presents a generalized power-decoupling control scheme using a multiport isolated bidirectional converter for multilevel inverter, which has multiple DC-links inside. In the proposed method, a single power-decoupling capacitor is needed for all the DC-links in the multilevel inverter cell. First, a prototype of the power-decoupling concept of individual H-bridge cells in the multilevel inverter is proposed, using a separate power-decoupling circuit. Then, a more advanced one-step power-decoupling method is proposed. The lifetime and reliability of the multilevel inverter is improved as film capacitors replace the large capacitance electrolyte capacitors. A multi-input ports/single output voltage-fed dual half bridge converter (MDHB) is used for the power-decoupling circuit. Steady state analysis for the peak and root-mean-square of the MDHB current is carried out for the loss breakdown. The currents are functions of the switching frequency, phase-shift, leakage inductance, turn ratio, and output voltage, which make the multiport transformer design complex. A design methodology is proposed that takes into account the design of the copper and core losses as functions of the switching frequency and number of turns. Furthermore, a special winding method for the input port is illustrated to obtain identical leakage inductances for the uniform current distribution in the multiport transformer. The proposed MDHB employs a current-sensorless power-decoupling control that contributes to the spontaneous ripple rejection of all the DC-links without individual link-current information, as well as to the cost and size reduction. Hence, the ripple-rejection controller is independent of the control configuration of the multilevel inverter, and also available for universal applications of various inverter topologies. Since the primary-input ports of MDHB share a single magnetic core for interfacing the ripple power to the unified secondary ripple capacitor, the controller design becomes difficult in considering the dynamic interaction among the ports, along with the average voltage-control loop design. In this paper, the dynamic analysis and controller design procedure of the circuit is also presented. The power-decoupling is achieved even when the ripple frequency is other than the double frequency of the inverter output, since the single-pole transfer function of the small-signal model of the MDHB allows sufficient phase-margin, along with high bandwidth. The proposed power-decoupling method for the multilevel inverter is validated with the help of simulation and 1.2-kW hardware-prototype experimental results.

Index Terms— Multilevel inverter, cascaded H-bridge inverter, multiport isolated converter, multiport transformer, and active power-decoupling

I. INTRODUCTION

Recently, power-electronics research has focused on utilization of renewable energy sources to replace fossil fuel, because of its
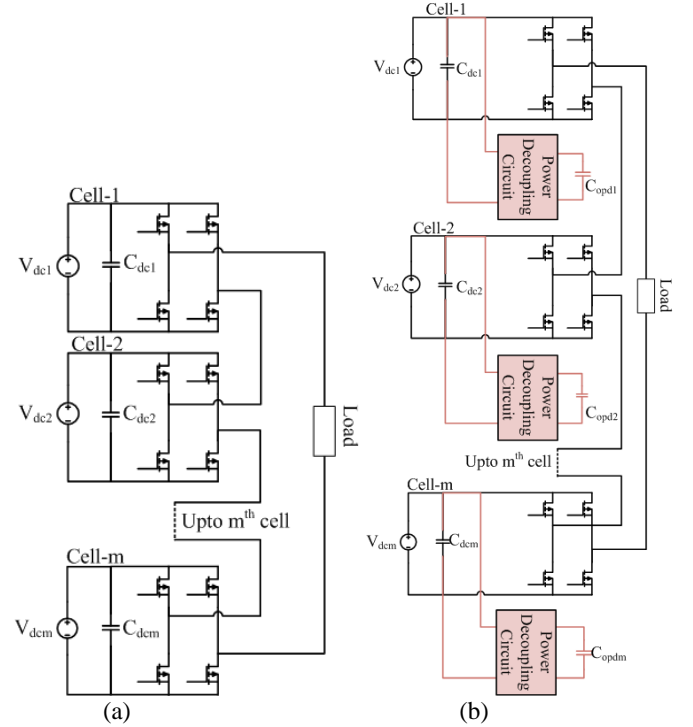

Fig. 1: Configuration of Power-decoupling in CHB Multi-level Inverter with (a) huge electrolyte capacitors ($C_{dc1}, \ldots C_{dcm}$), and with (b) small DC-link capacitors ($C_{dc1}, \ldots C_{dcm}$) of each cell by separate power-decoupling capacitors ($C_{opd1}, \ldots C_{opdm}$).

deleterious environmental effects. Since multilevel inverter and multi-port isolated converter topologies have a positive impact on using various renewable energy sources, and can achieve higher power and voltages with improved efficiency due to mature medium power semiconductor technology, they are beginning to attract attention for power electronics. The multilevel inverter topology with PV application is considered [1–2]. The adopted PV model is voltage source in series with a resistor. Compared to the conventional two-level type, multilevel inverters provide improved output signal quality, high voltage capability, reduced common mode voltages, low dv/dt , smaller or even no output filter, and large (nominal) power with low voltage rating semiconductors. The main research of the multilevel inverter naturally focuses on the improvement of the topologies and the control methodologies. Commonly used topologies of the multi-level inverters are the cascaded H-bridge inverter, and the neutral point clamped and flying capacitor [3–4]. For renewable energy systems, the cascaded H-Bridge inverter (CHB) is one of the most

commonly used topology among them. Figure 1 (a) shows that in the topology, every DC-link needs a huge electrolytic capacitor bank to absorb the ripple power from the H-bridge cells. In fact, the electrolyte capacitors reduce the lifetime and reliability of the multilevel inverter modules [5]. As a solution, an extra-circuited bidirectional power-flow power-decoupling technique has previously been suggested for conventional full-bridge inverters [6–8]. However, power-decoupling for multi-level inverters is rarely mentioned in the previous literature, because of the technical limitations. Figure 1 (b) shows that a separate power-decoupling circuit for an individual cell can be a feasible option for multi-level inverter power-decoupling solutions.

The problem with the configuration may be that the power-decoupling circuit becomes cost-ineffective and bulky in size, because of the multiple subsystem architecture, even though there is no report that objectively assesses this configuration for multi-level inverter power-decoupling through implementation. Therefore, a further advanced power-decoupling configuration for a multi-level inverter will be presented in this paper, which considers an integrated-type power-decoupling circuit for all the cells of the multi-level inverter.

Since no power-decoupling circuits for multi-level inverter have been reported so far, a literature review is conducted in this paper, based on power-decoupling for a single H-bridge inverter. Reference [9] mentions a power-decoupling concept for a multi-level inverter, but did not implement it experimentally. A symmetric half-bridge circuit is used as a power-decoupling circuit for a single inverter. Power-decoupling of the multi-level inverter by the symmetrical half-bridge bidirectional converter makes the power-decoupling circuit bulky and complex, because the same number of half-bridges as that of the main cells must be used for the CHB multi-level. A cell number of 'm' leads to m numbers of magnetic circuits (inductors) and twice (2m) the number of decoupling capacitors. Meanwhile in the proposed power-decoupling circuit, there is one magnetic circuit (multi-port transformer), and one decoupling capacitor. References [10–12] use a bidirectional buck-boost converter for power-decoupling of the single cell inverter. This also makes the power-decoupling circuit bulky, as in Ref. [9]. From the perspective of control, the voltage in Ref. [9] across the decoupling capacitor must have approximately $\pi/4$ phase-shift from the main inverter output voltage. The output filter of the inverter in Ref. [10] must be designed according to the supply frequency of the main inverter. The information of the inverter output current in Ref. [11] is needed for power-decoupling. Hence, the various power-decoupling controls of Refs. [9–11, 13] need information from the output of the main inverter. Due to these characteristics, they are all dependent on either the inverter's control, or the filter design; they therefore lose the capability of universal power-decoupling control for general multilevel inverters [14–15]. Whereas, the proposed power-decoupling control scheme requires no information from the inverter PLL and the filter(s), which makes the proposed power-decoupling control scheme universally applicable, and quite simple in design. The comparison between the proposed technique and buck-boost in [13] is in the following way. In the proposed power decoupling method, single power decoupling capacitor is used, however, in the buck-boost topology[13], three power decoupling capacitor would be used.

And, for each power decoupling capacitor in [13], voltage controller is needed whereas, in proposed power decoupling method, only one voltage controller is needed for power decoupling capacitor voltage. In proposed power decoupling method(current-sensorless control), there is no need of information from the multilevel inverter and in [13], current information and PLL from the inverter is required for power decoupling operation. It is the strong benefit of the proposed power decoupling control scheme and it makes the proposed power decoupling control scheme universally-applicable and quite simple design. The proposed power decoupling circuit is isolated which avoids the limitation on voltage across power decoupling capacitor whereas the buck-boost in [13] is non-isolated which restricts the voltage across power decoupling capacitor. The proposed power decoupling method needs one magnetic component, multi-port transformer, whereas in [13], three magnetic components, inductors, are required for three cells of the multi-level inverter. In the proposed power decoupling method, single power decoupling capacitor for all three cells of the multilevel inverter is 100µF on 200V DC-link for 1.2kW,60Hz system whereas in the buck-boost topology[13], the power decoupling capacitor for single cell is 200µF with 540V DC-link for 15kW, 233Hz system. For optimized size reduction and optimized voltage rating, the parameter, Kc,[21], is as in eq(1)below

$$K_c = \frac{\frac{1}{2} f_{line} C V_p^2}{P} \qquad (1)$$

Where, f_{line}- line frequency, C- power decoupling capacitance, V_p- peak voltage across power decoupling capacitor and P- rated power. The parameter, K_c, indicates the volume of the power decoupling capacitor per unit energy.   For the buck-boost topology[13], it is $314.6 * 10^{-3}$ while for the proposed power decoupling method, it is $196 * 10^{-3}$. Therefore, proposed power decoupling method has benefit of size reduction with lower voltage rating over the buck-boost topology [13].   It is summarized in the following Table I.

From the perspective of cost, Refs. [10, 12] require the information of the DC-link voltage, input current to the inverter, and voltage across the power-decoupling capacitor per H-bridge. This leads to m number of current sensors, and twice the number of voltage sensors for power-decoupling in the CHB (m-cell) multilevel inverter. Whereas, the proposed power-decoupling control scheme is current-sensorless, and it needs only the voltage information of each DC-link and the decoupling capacitor. Therefore, the proposed power-decoupling control scheme only requires m+1 number of voltage sensors, which makes the proposed power-decoupling control scheme very cost-effective. The number of sensors required for Ref. [9] is higher than that of the proposed power-decoupling control scheme. In Refs. [9–12], an average voltage control loop for every power-decoupling cell is required. Whereas in the proposed control scheme, only one average voltage control loop is required for power-decoupling of the entire cells of the multi-level inverter. This makes the proposed control scheme simpler, and more cost effective.

Table I. Comparison of the proposed and conventional power decoupling methods

S.No.	Proposed Technique	Buck-boost [13]
1	It provides isolation among the ports	It doesn't provide isolation
2	By means of isolation, there is no limitation on choosing average voltage across power decoupling. Therefore, voltage swing across power decoupling capacitor is not restricted	In buck-boost power decoupling circuit, the average voltage across the power decoupling capacitor can be higher or lower than the dc link voltage. It restricts the voltage swing across the power decoupling which limits the power decoupling capability.
3	It needs one integrated magnetic component(multi-winding transformer)	It requires three magnetic components(three inductors)
4	It requires one power decoupling capacitor	It requires three power decoupling capacitors and hence voltage controller for each power decoupling capacitor.
5	No information is needed from multilevel inverter outputs for power decoupling control scheme. It makes proposed power decoupling control simple.	It requires information from the inverter's PLL for power decoupling control scheme. It makes the power decoupling control more complex.
6	Volume of power decoupling capacitor per unit energy is lower as compared to [11]($K_c = 196 * 10^{-3}$)	Volume of power decoupling capacitor per unit energy is higher than the proposed technique. ($K_c = 314.6 * 10^{-3}$)

From the perspective of capacitor design, all of the conventional power-decoupling circuits are of the non-isolated type, which leads to a limitation of the voltage range across the decoupling capacitor ($C_{opd1}, \dots C_{opdm}$). Because of this limitation, the decoupling capacitance cannot be effectively reduced, as it depends on the average and swing voltage. The proposed power-decoupling circuit is an isolated type that is free from the step-up or -down of the voltage range. The following sections discuss the research challenges, the proposed circuit, contributions of the paper and the paper outline.

A. Motivational and Technical Challenges

The motivation of the paper is to propose a power-decoupling method for a multilevel inverter with single power-decoupling capacitor. Using a large capacitance electrolytic power-decoupling capacitor for every cell increases the size and cost, and also decreases the reliability and lifetime of the circuit [16–20]. Furthermore, by using a separate power-decoupling cell for each multilevel H-bridge, individual feedback control loops with separate voltage and current sensors are needed for every power-decoupling cell, which adds complexity and cost. Therefore, a multi-input ports / single-output topology is supposed to provide an ultimate solution to link the ripple power from every DC-link to a single power-decoupling capacitor. In the multi-port topology, isolation among the ports is the primary requirement. In consequence, a multi input ports/ single output isolated bidirectional topology is necessary to transfer all of the DC-link ripple power to the secondary-side decoupling capacitor. The bidirectional dual half bridge (DHB) is considered in this paper, whereas other bidirectional isolated topologies can also be used [21]. However, the multi-port transformer design is a technical challenge, as the currents through the multi-port transformer are dependent on many factors, such as the leakage inductance, switching frequency, output voltage, and the PWM phase-shift. The transformer design process requires details of the current RMS equation to be developed for loss analysis. Secondly, one of the main challenges in the design process is to make a uniform current distribution among the DC-link ports, by ensuring leakage inductances similar as much as possible. This similar leakage inductances requirement is preferable to have similar currents' distribution in the input ports for balancing the currents (heating) through the primary windings.

One more challenge in the design is to block the power-flow interaction among the input DC-link ports. Another challenge for obtaining the power-decoupling application in the multi-level inverter is the control scheme. The control scheme should be able to efficiently transfer the ripple power from each of the DC-links of multi-level inverter cells to the power-decoupling output port. In particular for universal application of the power-decoupling control scheme, a further challenge exists, namely the elimination of the synchronization with inverter Phase-Lock-Loop (PLL). This is essential to guarantee that the controller will operate well with various kinds of multi-level inverter topologies or PWM methods, when the PWMs of the multi-level inverter cells are not in-phase with the main inverter.

Finally, the input ports of the transformer are magnetically coupled in a magnetic core, and that increases the complexity of the challenge in the transient analysis to design the capacitor voltage power-decoupling controller.

B. The Proposed Circuit and Control Methodology

Figure 2 shows the proposed power-decoupling circuit for the m-cell multi-level inverter. The power-decoupling circuit has m number of input ports, input port 1, input port 2, …, and input port m, which are connected to the corresponding m DC-links of the multilevel inverter, DC-link-1, DC-Link-2, …, DC-Link m. The input ports of the power-decoupling circuit are linked with the power-decoupling output port by the same magnetic core. Each input port and the power-decoupling port are regulated by a dual half-bridge (DHB) bidirectional phase-shift converter. The power decoupling port is connected to a power decoupling non-electrolytic capacitor.

With the help of the proposed power decoupling method, all of the DC-links' ripple powers are collected at the output power-decoupling port, in the power stage. The DC-links' ripple powers are then transferred to the power-decoupling port by the phase-shift modulated between the input and output ports and the voltage-feedback control scheme. Therefore, the power decoupling capacitor has to decouple the aggregated double frequency ripple power. Therefore, the capacitance, Cd, required for the power decoupling for power, P, is given by eq(2) [21] as below:

$$C_d = \frac{P}{2\pi f_{line} V_{opd} \Delta V_{opd}} \qquad (2)$$

Where, V_{opd} is the average voltage, ΔV_{opd} is the voltage ripple across the decoupling capacitor, P is the multilevel inverter output power and fline is the line frequency of the multilevel inverter (60 Hz in this case).
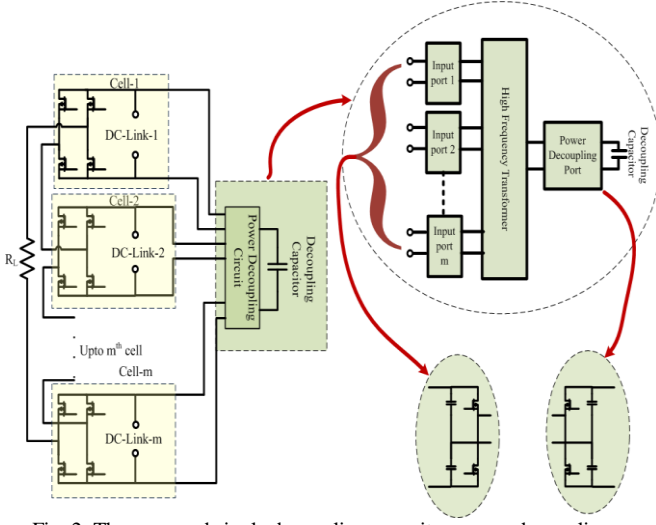

Fig. 2: The proposed single decoupling capacitor power-decoupling circuit for a cascaded H-bridge multi-level inverter.

In the proposed topology, the total decoupling capacitance is 100µF in the output of the power decoupling circuit for power rating of 1.2 kW. This is with V_{opd}=200 V, ΔV_{opd}=160 V and 10 % voltage ripple in the DC-link voltage. Whereas, with the conventional method, the total decoupling capacitance is 795.8 µF for all the three cells of the multilevel inverter i.e each DC-Link should have 265.3 µF for 200-V DC-link voltage with 10 % voltage ripple. This is not taking into account ripple current capabilities as film capacitors have higher ripple capabilities. Therefore, with the proposed power decoupling method, the decoupling capacitance is reduced by 7.96 times.

The transformer gives an additional design freedom for the voltage-swing range of the decoupling capacitor, which contributes to the capacitance reduction at the output. The similar current (or heat) distribution in the primary windings of the transformer (or input ports) is achieved by having the leakage inductances similar as much as possible. This requirement of similar leakage inductances is not a necessity for the proposed power decoupling method.

Although this paper is concerned with single-phase topology, the proposed method is more effective with three-phase systems. In a three-phase system, the power-decoupling capacitor can be further reduced.

The proposed power decoupling control scheme is based on voltage dynamics and it has one ripple rejection loop for each port and one average voltage control loop for regulating average voltage across power decoupling capacitor. The single pole behavior of proposed circuit gives the simple control and, also, the high bandwidth of ripple rejection controller can be achieved. The proposed control scheme is dependent on voltage dynamics with optimal number of voltage sensors. There is no need of complex DC-link voltage reference estimation of each cell in the multilevel inverter. The proposed power decoupling control scheme has the advantage of requiring no information from the multilevel inverter and it makes the proposed power decoupling method to be applicable to any kind of inverter architecture.

C. Contribution

This paper presents a solution for multilevel inverter power-decoupling circuits to eliminate electrolytic DC-link capacitors. A multi input-port / single-output bidirectional voltage-fed DHB converter is proposed as the power-decoupling circuit. The contributions of the paper are summarized as: (1) A single power-decoupling capacitor is proposed for power-decoupling of all the multi-level inverter cells. The ripple power, generated in all of the DC-links of multi-level inverter, is coupled by a single power-decoupling capacitor at the output port by a multi-input ports/single-output transformer of an isolated bidirectional converter. (2) Design-oriented steady-state analysis for the multi-input port / single-output dual half-bridge is carried out, based on the fact that the peak and RMS currents in the converter are dependent on many factors, like switching frequency, phase-shift, leakage inductance, turn ratio, and output voltage. In the analysis, RMS current equations are obtained for the purpose of optimizing the losses. (3) A design methodology for the optimal power distribution in the multi-winding transformer is presented. For uniform power distribution among the windings, similar currents in the input ports are required. From the operating principles of the phase-shift DHB topology, similar leakage inductances are desirable. Therefore, a method to wind the input ports' windings is discussed to obtain similar leakage inductances. (4) Since the input ports of the converter share a common magnetic core, the transient analysis process becomes challenging for the design of the output voltage controller. Hence, the controller-design for multilevel inverter power-decoupling is also developed in this paper, and (5) a generalized power-decoupling control scheme is presented for the multi-level inverter. The proposed power-decoupling control scheme is of the current-sensorless type. The current-sensorless configuration offers the advantage that it needs no information from the main inverter, even the PLL. An average voltage power-decoupling controller is used for all the ripple-rejection loops. The single-pole characteristic of the small-signal transfer function of the multi-port DHB converter makes it more suitable for the design of a high-bandwidth ripple-rejection control loop. The proposed power-decoupling controller ensures power-decoupling performance, even when the ripple power at the DC-link of multi-level inverter cell is higher than the double frequency.

The contributions of the paper mentioned above make the proposed concept a promising and advanced configuration for multilevel inverter power-decoupling.

D. Paper Outline

This paper is organized as follows: Section II describes the steady-state analysis multi-port DHB. Section III then carries out a multi-port transformer design. Section IV gives the details of the transient analysis and controller design. Section V presents the simulation and experimental results for verification of the proposed multi-level inverter power-decoupling method. Finally, Section VI concludes the paper.

II. STEADY-STATE ANALYSIS OF THE MULTI-PORT DHB

As aforementioned, the multi-port DHB converter has a multi-port transformer that needs careful design consideration to achieve a converter with feasible efficiency. The efficiency is optimized by reducing dominant losses in the transformer.

Therefore, steady-state analysis of the converter is carried out to obtain the RMS currents' expression through the design parameters of the multi-port transformer.

Figure 3 shows the power stage diagram of the multiport bidirectional DHB converter. In the figure, the voltage sources, Vin-m, each with the resistance, R_{in-m}, are taken as power sources for each cell of the multilevel inverter. In Fig. 3, V_{dc-1}, V_{dc-2}, …, V_{dc-m} represent the DC-link voltages of each port of the converter, i_{L1}, i_{L2}, …, i_{Lm} represent the currents through the input port of the multi-port transformer, V_{p1}, V_{p2}, …, V_{pm} mean the voltages across the input port windings, L_{p1}, L_{p2}, …, L_{pm} represent the leakage inductance of the multiport transformer, n_{p1}, n_{p2}, …, n_{pm} represent the number of turns of the input port windings, n_s represents the number of turns in the output port winding, and V_{opd} represents the output voltage, respectively.

The power transfers between each input (P_{oi}) and an output port, or between the input ports (P_{ik}), are dependent on phase-shift, leakage inductance, and the turn ratio. The power transfer can be realized from the power transfer equations given in Eqs. (3) and (4):

$$P_{oi} = \frac{V_{dc-i}V_{opd}}{8\pi^2 nL_{pi}f}\varphi_i(\pi - |\varphi_i|) \ , i = 1,2 \ldots m \qquad (3)$$

$$P_{ik} = \frac{V_{dc-i}V_{dc-k}}{8\pi^2 nL_{pik}f}\varphi_{ik}(\pi - |\varphi_{ik}|) \ ; i,k = 1,2 \ldots m \qquad (4)$$

where, V_{dc-i} is the input port voltage of the ith port, V_{dc-k} is the input port voltage of the kth port, V_{opd} is the output voltage, L_{pi} is the leakage inductance of the transformer referred to the corresponding input port side of the transformer, L_{pik} is the

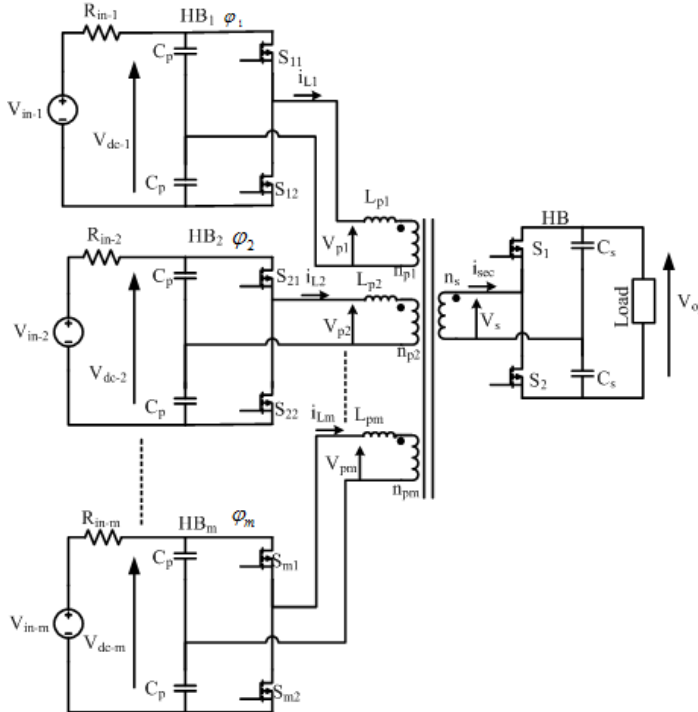leakage inductance between the ith and k^{th} port referred to the ith

port, f is the switching frequency, φ_{ik} is the phase-shift between the ith and k^{th} port, and φ_i is the phase-shift of the output port with respect to the input port. Equation (4) clearly shows that the DHB topology is based on the phase-shift control, as the power is dependent on the phase-shift. Since there is a chance of power transfer between the input ports, the controller maintains the switching in-phase among the input ports. Then, the total output power becomes Eq. (5):

$$P_o = \sum_{i=1}^m P_{oi} \qquad (5)$$

The phase shift for every port has its own phase shift which could be different from other ports. Every phase shift is controlled by for ripple rejection in its corresponding port. However, for simplification of steady-state analysis, the phase shift angles for every port are assumed to be equal. The key waveforms are shown in fig.4 with equal phase shift i.e $\varphi_1 = \varphi_2 = \varphi_3 = \varphi$. The multi-port DHB converter has four operating modes. The duty cycle is taken as 0.5 for balancing of the capacitors. The
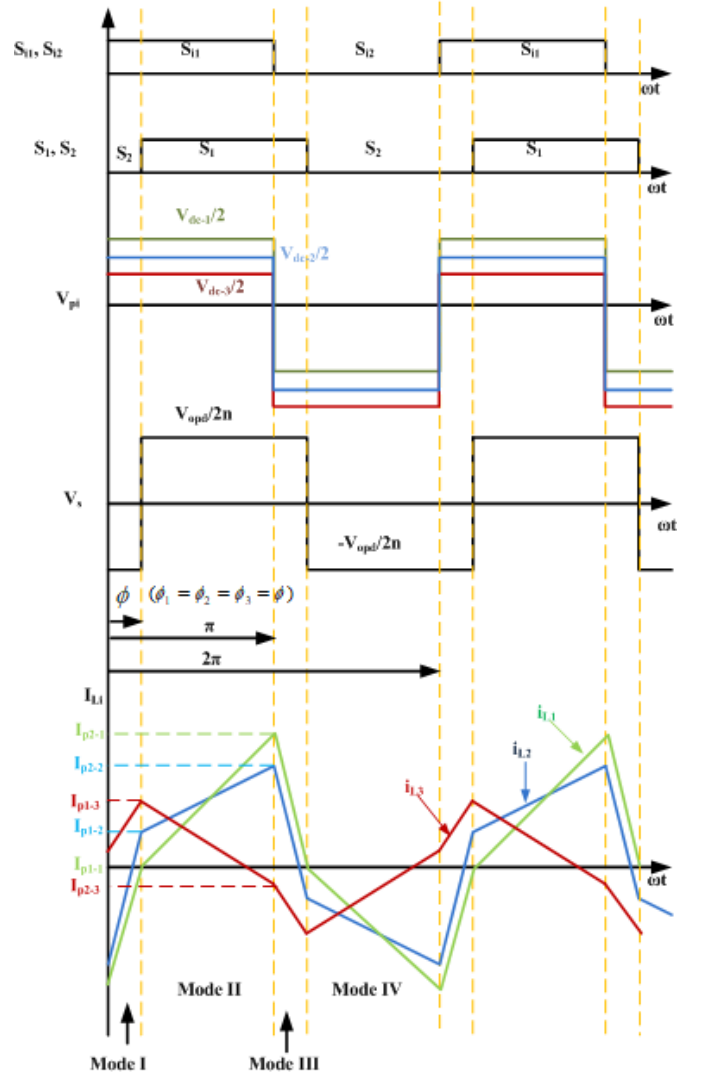

Fig. 4: Key waveforms for the multi-port DHB converter with $\varphi_1 = \varphi_2 = \varphi_3 = \varphi$, $V_{dc-3} < \frac{V_{opd}}{n} < V_{dc-2} < V_{dc-1}$.

Fig. 3. Power-stage circuit diagram of the multi-port bidirectional DHB converter.

currents through the multi-port transformer are dependent on the leakage inductance, switching frequency, phase-shift, output voltage, and turn ratio. The current shape changes to the voltage relationship between the input voltage to the primary side, Vdc-i, and the output voltage, Vopd (in Fig. 3). Ipa-i and Ipb-i are the currents at the end of I mode and II mode, respectively. Equation (6) gives the expressions for the currents:

$$\left. \begin{array}{l} I_{pa-i} = \frac{2\phi - \pi}{4\omega L_{pi}} V_{dc-i} + \frac{\pi}{4\omega n L_{pi}} V_{opd} \\ I_{pb-i} = \frac{\pi}{4\omega L_{pi}} V_{dc-i} + \frac{2\phi - \pi}{4\omega n L_{pi}} V_{opd} \end{array} \right\} \quad i = 1,2\ldots m \ (6)$$

Equation (6) makes clear that when V_{dc-i} is greater than V_{opd}, the peak current of the transformer is I_{pb-i}. When V_{opd} is greater than V_{dc-i}, the peak changes to I_{pa-i}. This also implies that the peak current of the transformer is dependent on the voltage difference of the input and output voltage. The currents, I_{pa-i} and I_{pb-i}, are also inversely proportional to the leakage inductance and the frequency. For fair distribution of current among the input port windings, Eq. (6) implies that the leakage inductances should be identical for the same power transfer, as the DC-link voltages of all of the input ports are equal.

Avoiding the complex expression for RMS current through the transformer primary side, I_{Lrms-i}, the RMS current, I_{Lrms-i}, is obtained in terms of I_{pa-i} and I_{pb-i}. The instantaneous currents through the primary side of the transformer are obtained for each mode as:

Mode I
$$i_{L-i}(\omega t) = \frac{I_{pa-i} + I_{pb-i}}{\varphi_i}\omega t - I_{pb-i} = i_{1-i}(\omega t); \quad i = 1,2\ldots m \ (7)$$

Mode II

$$i_{L-i}(\omega t) = \frac{(I_{pb-i} - I_{pa-i})}{\pi - \varphi_i}(\omega t - \varphi_i) + I_{pa-i} = i_{2-i}(\omega t);$$
$$i = 1,2\ldots m \quad (8)$$

From the waveform of i_{L-i} in Fig. 4, the RMS expression of i_{L-i} can be written as:

$$I_{L-i}^2 = \frac{1}{\pi}\left[\int_0^{\varphi_i} i_{1-i}^2(\omega t)d\omega t + \int_{\varphi_i}^\pi i_{2-i}^2(\omega t)d\omega t\right] \quad ; \quad i = 1,2\ldots m \ (9)$$

From Eqs. (7), (8), and (9),

$$\int_0^{\varphi_i} i_{1-i}^2(\omega t)d\omega t = \frac{(I_{pa-i} + I_{pb-i})^2}{\varphi_i^2}\left(\frac{\varphi_i^3}{3}\right) + I_{pb-i}^2\varphi_i - \frac{I_{pb-i}}{\varphi_i}(I_{pb-i} + I_{pa-i})\varphi_i \quad ; \quad i = 1,2\ldots m \quad , \quad (10)$$

And,

$$\int_{\varphi_i}^\pi i_{2-i}^2(\omega t)d\omega t = I_{pa-i}^2(\pi - \varphi_i) + \frac{(\pi - \varphi_i)}{3}(I_{pb-i} - I_{pa-i})^2 + (\pi - \varphi_i)I_{pa-i}(I_{pb-i} - I_{pa-i}) \quad ; \quad i = 1,2\ldots m \ (11)$$

On substituting Eqs. (10) and (11) into Eq. (9), the transformer primary RMS current is obtained as in Eq. (12):

$$I_{Lrms-i} = \sqrt{\frac{1}{3\pi}\left\{ \begin{array}{l} (3\pi - 2\varphi_i)I_{pa-i}^2 + \varphi_i(I_{pb-i}^2 - I_{pa-i}I_{pb-i}) + \\ (\pi - \varphi_i)(I_{pb-i} - I_{pa-i})(I_{pb-i} + 2I_{pa-i}) \end{array} \right\}}$$
$$i = 1,2,\ldots, m \ (12)$$

The expression for the transformer secondary side current is as in Eq. (13):

$$I_{sec-rms} = \frac{1}{n_s}\sum_{i=1}^m n_{pi} I_{Lrms-i} \quad (13)$$

From Eq. (12), the transformer RMS current can be limited by I_{pa-i} and I_{pb-i}. Therefore, I_{Lrms-i} and $I_{sec-rms}$ are functions in leakage inductance and the switching frequency for the same power level. This dependency of the currents makes the conduction losses dependent on the switching frequency.

III. LOSS ANALYSIS

A. Multi-Port Transformer Design

The conventional transformer design is based on the RMS current, number of turns in the windings, switching frequency, and expected loss limit, and the current through the transformer generally, not depending on the switching frequency. However, in the multi-port DHB converter, since the transformer currents are dependent on the switching frequency, the conduction losses in the multi-port transformer also become dependent on the frequency. Hence, the multi-port transformer is not straight-forward, but very complicated. Figure 5 summarizes the design process in a flowchart. In the design process, the power, DC-link voltage, output voltage, and expected loss limit in the transformer are first defined. In the multi-port DHB converter, because the currents can be different with switching frequency variation, even for a fixed power capacity, a range of switching frequency is chosen to minimize the losses. Then, the phase-shift is calculated to have the rated power. With respect to the calculated phase-shift and the switching frequency, the RMS currents of all windings are obtained. The range of number of turns is selected based on the inductance. Then, the limit value of the magnetic flux density of the chosen core is checked. If the magnetic flux density is within the limit, then the copper and core losses (P_{L-iter}) are calculated, in order to compare and find the minimum value. If the magnetic flux density is out of the limit, then the core size is updated, so that it can withstand the maximum magnetic flux density. In this manner, the total losses are obtained for the entire range of the switching frequency and number of turns, and the minimum loss found with the corresponding switching frequency and number of turns.

In the multi-port transformer, the copper loss equation is as below:

$$P_{cu} = \frac{\rho(MLT)}{W_a K_u} n_{p1}^2 I_{trms}^2 \quad (14)$$

where, ρ is the resistivity of wire, MLT means the length per turn, W_a is the core window area, K_u is the winding fill factor, n_{p1} is the number of turns in the input port 1 winding, and I_{trms} the total sum of the RMS current of all windings referred to the input port 1 winding. The sum of the RMS current of all the windings referred to input port 1 winding is given by eq. (15):
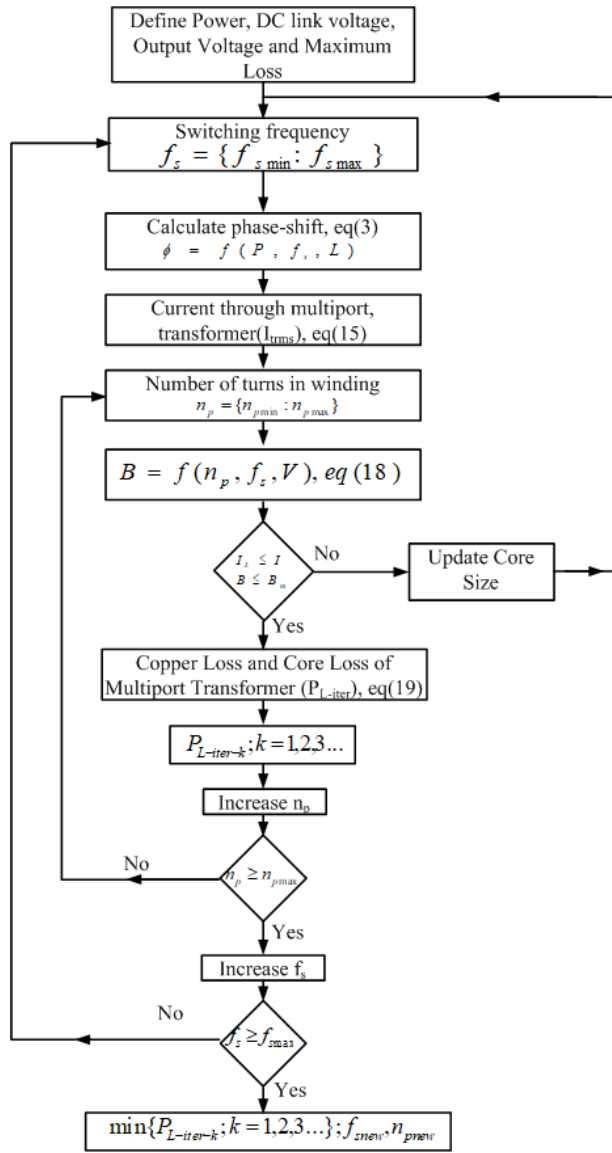
Fig. 5: Flowchart of the multi-port transformer design process according to the loss constraint.

$$I_{trms} = \sum_{i=1}^{m} \frac{n_{pi}}{n_{p1}} I_{Lrms-i} + \frac{n_s}{n_{p1}} I_{sec-rms} \qquad (15)$$

The core loss is given in eq. (16):

$$P_{core} = af^x B^y L_t A_c l_m \qquad (16)$$

where, B is the magnetic flux density, A_c is the core cross-section area, l_m is the mean magnetic length, a = 3.5, x = 1.4, y = 2.5, and L_t is given by eq. (17):

$$L_t = \begin{array}{ll} b - cT + dT^2 & for\ all\ other\ temperatures \\ 1 & for\ T = 100\ ^\circ C \end{array} \Big\} \qquad (17)$$

b= 0.88, c = 0.013, and d = 0.000142, and T = 50 °C.

Then, the core size of the multi-port transformer is obtained by optimizing the flux density [22]. The flux density B(t) is optimized by the number of turns and switching frequency as eq. (18):

$$B(t) = \frac{1}{n_{pi}A_c} \int v(t)dt \qquad (18)$$

So, the total Loss, P_L, is obtained as in eq. (19):

$$P_L = P_{core} + P_{cu} \qquad (19)$$

The equations show that the conduction loss in the multi-port transformer is minimized by the number of turns in the windings and the switching frequency, as the RMS currents are dependent on the switching frequency through the multi-port transformer. For consideration of the complex dependency of the copper loss on switching frequency and the number of turns, contour plots of their relationships are obtained. Figure 6 shows the contour plot. The plot shows that the innermost contour is the lowest total loss region in the design procedure. So, the red dotted line means a set of the lowest number of turns at a specific switching frequency. Hence, the number of turns on the dot is recommended for the optimal copper design. In this paper, the design specification of the switching frequency for the hardware experiment was 30 kHz, and the number of turns was selected as 50, as shown in the figure. The frequency was fixed, to avoid a resolution problem of the digital controller (TMS28335, Texas Instrument). Since the DHB controller operates based on the phase-shift control among the legs, 1° phase-shift of the 30-kHz PWM corresponds to 0.092 μsec, which is shorter than the 2-clock time-span of the 18-MHz DSP. So, a higher frequency than this is impractical for implementation of the DHB converter. If a high clock-speed DSP can be used, then the switching frequency can also be enhanced. From the figure, it is supposed that the total loss with 30 kHz
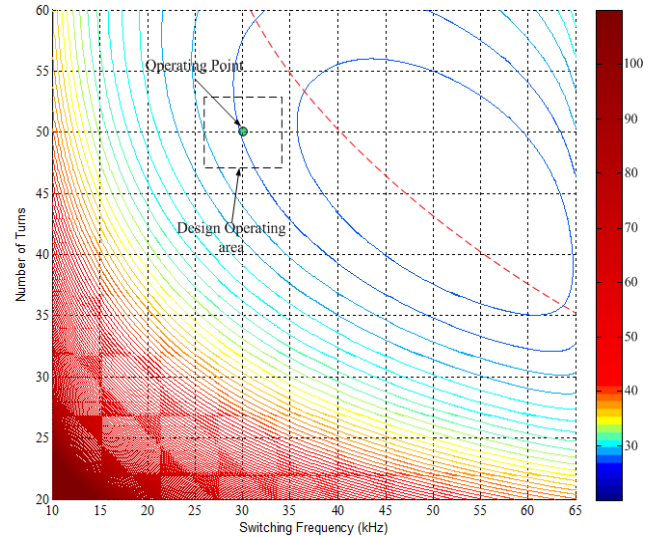

Fig. 6: Design contour of the total transformer loss (P_L) vs. number of turns in the input port 1 winding (n_{p1}), and switching frequency (f_s).

would be in the range of 2% of the total output power.

The multi-port DHB converter is also supposed to have an equally distributed power transfer from the individual ports to the output, due to the power delivery characteristic of the symmetric cascaded H-bridge multi-level inverter. So, to guarantee a uniform loss distribution in the multi-port transformer, the

average current through each winding should be uniform for identical power transfer from each input port to the output port. For the current uniformity of the multi-port DHB converter, the leakage inductance of each winding should be identical, as the winding currents are dependent on the corresponding leakage inductance. Therefore, a similar leakage inductance of each input port winding of the multiport transformer is a mandatory design requirement for uniform loss distribution in the multiport transformer. The methodology described to achieve equal or similar leakage inductances in the transformer is not a necessity for the proposed power decoupling circuit. Proposed power decoupling circuit works with other winding methods for multiport transformer. The methodology for obtaining the similar leakage inductance of the transformer is based on having similar flux leakage of each primary winding with respect to the secondary winding of the transformer. For similar flux leakage of the primary windings with respect to the secondary winding, the geometry of each primary winding with respect to secondary winding should be similar. For having the similar geometry of the primary windings with respect to the secondary winding, the primary windings of the transformer are twisted.

Figure 7 shows the particular manner in which the input windings are wound for similar inductances. First, the input port windings are transposed to each other, as shown. However, the transposing of the windings may give rise to insulation breakdown, due to proximity and heating in the winding. This problem can be avoided by using a heat-shrink tube surrounding each winding, to secure the necessary distance. The bundle of the transposed input ports windings are then wound around the core. Figure 8 shows the produced-in-lab multi-port transformer. By transposing the input port windings, the obtained leakage inductances are 32, 35, and 37 µH, which are close enough to one another to conform to the symmetry power handling.
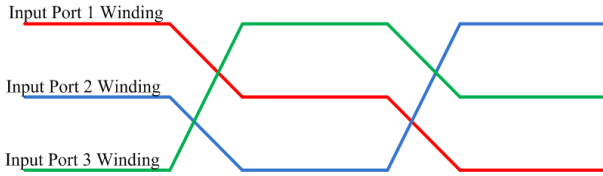

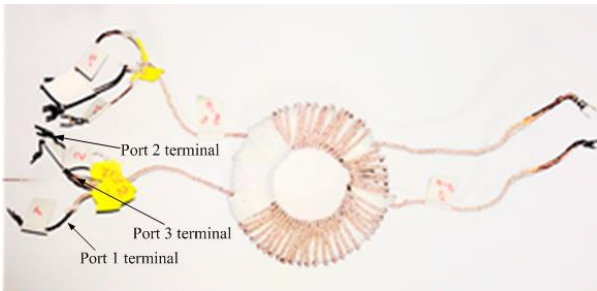Fig. 7: Input ports' winding transposition.

Fig. 8: Multi-port Transformer for the hardware prototype.

B. Half-Bridge Loss Analysis

For consideration of the transistor bridge losses, there are switching and conduction losses. The switching losses in the transistor bridge are considered as negligible because of the capability of zero voltage switching operation in dual half-bridge topology. Therefore, significant losses in the transistor bridge are the conduction losses. The conduction losses in the bridge are

considered in the following way. The transformer primary-side current and switch current waveforms are shown in fig. 9.
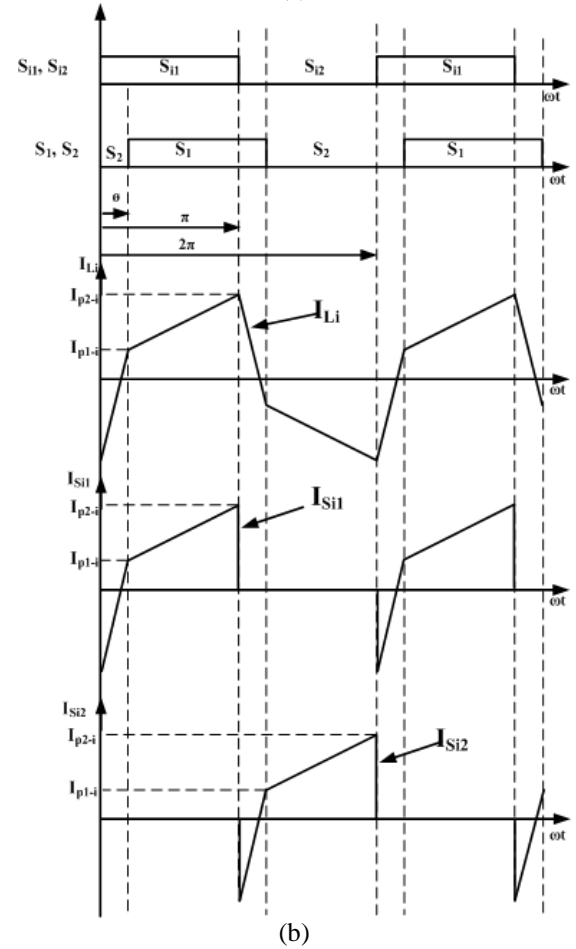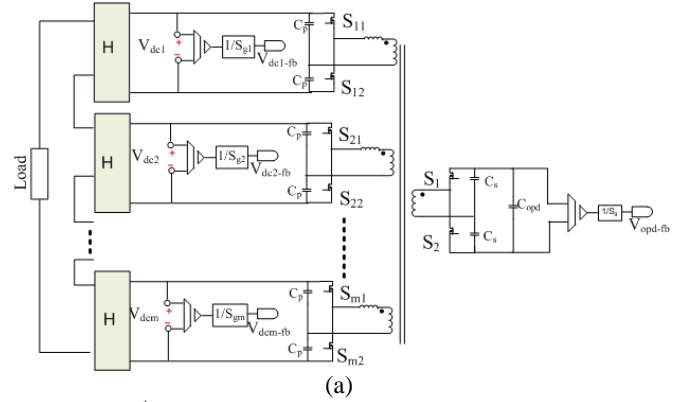

(a)

(b)

Fig.9: (a)Schematic diagram and (b) Transformer primary-side current and high-side and low-side switch currents waveform

The high-side switch current, I_{si1}, and low-side switch current, I_{si2}, can be related to the transformer current as in eq.(20)

$$I_{si1} = I_{si2} = \sqrt{2}I_{Li} = I_{sw} \tag{20}$$

Therefore, the conduction losses in one transistor bridge is as in eq (21)

$$P_{sw} = 2I_{sw}^2 r_{DSon} = I_{Li}^2 r_{DSon} \tag{21}$$

where, r_{DSon} represents switch resistance.

The conduction loss, P_t, including corresponding transformer winding resistance, r_t, is as in eq. (22)

$$P_t = I_{Li}^2(r_{DSon} + r_t) \tag{22}$$

From eq. (22), the switch resistance, r_{DSon}, is neglected because it is very small as compared to the winding resistance, r_t.
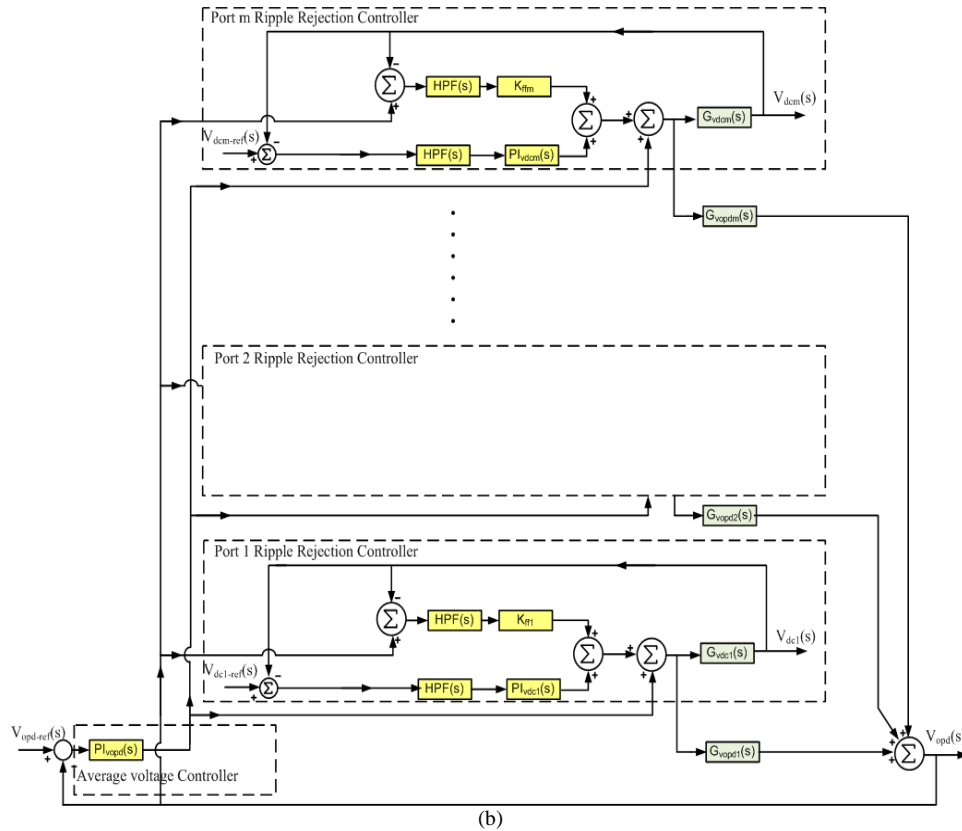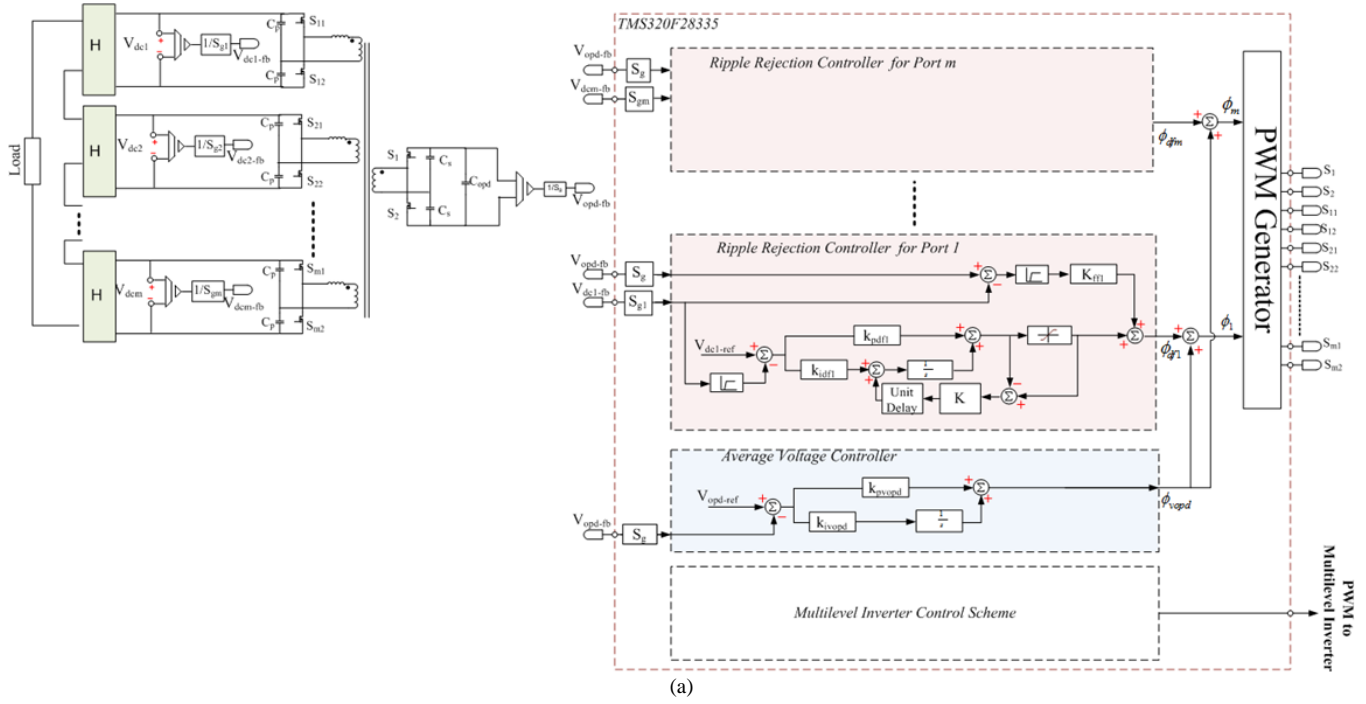

(a)

(b)

Fig. 10 (a) : Physical schematic diagram for proposed single-capacitor power-decoupling control scheme for m-number of H-bridge multilevel inverter and (b) Mathematical small-signal model for proposed single-capacitor power decoupling control scheme for arbitrary (m) number of input ports.

$$P_t = I_{Li}^2 r_t \ as \ r_t \gg r_{DSon} \qquad (23)$$

The switch resistance can also be considered by eq. (22), however in our case, since the switch resistance is very small as compared to the winding resistance, it is neglected. The transformer current is minimized by design algorithm of the transformer. Hence, the losses are minimized.

IV. Control Methodology and Design

In this section, the proposed control methodology and control design is discussed. These are as followings.

A. Control Methodology

Figure 10 shows the controller configuration of the proposed power-decoupling scheme for the multi-level inverter. The figure shows the ripple-rejection control loop for each cell of the multilevel inverter, and also shows one average-voltage controller regulating the voltage across the output power-decoupling capacitor. The proposed power-decoupling control scheme is based on the voltage dynamics only, i.e., a current-sensorless type. In the ripple rejection controller, the instantaneous DC-link voltage (V_{dc1} to $V_{dc,m}$, respectively) is fed to a PI compensator, and compared with a zero reference, after the DC-component is filtered by a high-pass filter. The zero regulation means the elimination of the entire AC component, including the DC-link double-frequency voltage ripple. An anti-winding up controller is shown, which is to avoid the saturation of the PI controller. The current-sensorless control is possible due to the inherent fast (one-pole) dynamic characteristics of the DHB converter topology. The ripple rejection controller includes an auxiliary feed-forward controller, instead. So, the proposed controller is a voltage-fed feedback-feedforward hybrid type.

The proposed power decoupling control scheme has two controllers one is for ripple rejection and other for maintaining the average voltage across power decoupling capacitor. The ripple rejection controller consists of PI controller and feed-forward controller. In fig. 10, the ripple rejection controller removes, besides the double frequency component, other frequencies above 20Hz too. Resonant controllers can also be used in the proposed power decoupling control scheme, however with some multilevel inverter, the frequency components available at DC links are not pure double frequency component, i.e. it could have higher or lower frequency components at the DC links. Therefore, the proposed power decoupling controller is more generalized one.

All the design parameters of the ripple rejection controllers are such as k_{pdfi}, which represents the proportional controller gain, and k_{idfi}, which represents the gain of integral one, with two high-pass filters. In the average voltage controller, k_{pvopd} represents the gain of the proportional controller, and k_{ivopd} represents the gain of integral one. Since all the feedback information is from the DC-link node, not from the inverter, the proposed power-decoupling control scheme is independent of the control configuration of the following multi-level inverter. It is a serious advantage for the proposed controller scheme, because the feature enables the power-decoupling circuit to apply universally to any kind of inverter topology /architecture. Furthermore, operation without a current-feedback controller avoids the complex DC-link voltage-reference estimation of each cell in the multilevel inverter, which adds a strong benefit to the controller design process, which is simplified by the decoupled main-inverter and power-decoupler controllers. Finally, conventional schemes require a two-loop controller, one loop for suppressing the double frequency voltage ripple, and the second loop for controlling the average voltage

across the power-decoupling capacitor. So, the total number of loops required for the m-cell multilevel inverter is 2m. In

Table II. Key parameters for the controller design.	
CIRCUIT PARAMETERS	VALUE
Output Power	1.2 kW
Decoupling Capacitor voltage	200 V
DC-Link Voltage	200 V
Phase-shift	34 Deg
Leakage Inductance of the port L_{pi}	32 µH
Inductor on secondary side of the transformer L	13 µH
C_{pi}	50 µF
C_s, C_{opd}	50 µF, 75 µF
Transformer's winding turns	56 / 50
Equivalent source resistance R_{in}	20.6 Ω

comparison, the proposed scheme requires m + 1 number of loops, composed of m-number of loops for the double frequency voltage-ripple reduction, and one control loop for controlling the average voltage. This feature contributes to the simplified design process and low manufacturing cost.

B. Control Design

Since the proposed power-decoupling control scheme is based on the voltage dynamics only, the transient analysis includes the DC-link voltage dynamic response. Also, the multilevel inverter uses a phase-shifted PWM modulation. So the small-signal transfer functions for the DC-link and average-capacitor-voltage from the phase-shift are given as eqs. 24(a) and 24(b) [21]:

$$\frac{\tilde{v}_{dc}}{\tilde{\phi}} = -\frac{\frac{V_{34}(\pi - 2\phi)}{2\pi\omega L C_p}\left(s + \frac{2}{R C_s'}\right) + V_{12}\phi\frac{(\pi - \phi)(\pi - 2\phi)}{(2\pi\omega L)^2 C_p C_s'}}{s^2 + 2\left(\frac{1}{R_{in}C_p} + \frac{1}{R C_s'}\right)s + \frac{1}{C_p C_s'}\left(\frac{\phi(\pi - \phi)}{2\pi\omega L}\right)^2 + \frac{4}{R_{in}C_p R C_s'}} = G_{vdc-i}(s)$$

(24a)

$$\frac{\tilde{v}_{opd}}{\tilde{\phi}} = \frac{\frac{V_{12}(\pi - 2\phi)}{2\pi\omega L C_s'}\left(s + \frac{2}{R_{in}C_p}\right) - V_{34}\phi\frac{(\pi - \phi)(\pi - 2\phi)}{(2\pi\omega L)^2 C_p C_s'}}{s^2 + 2\left(\frac{1}{R_{in}C_p} + \frac{1}{R C_s'}\right)s + \frac{1}{C_p C_s'}\left(\frac{\phi(\pi - \phi)}{2\pi\omega L}\right)^2 + \frac{4}{R_{in}C_p R C_s'}} = G_{vopd}(s)$$

(24b)

Figure 10(b) shows the mathematical small-signal model for proposed single-capacitor power decoupling method for arbitrary (m) number of input ports. The design procedure is performed with the system parameters given in Table II. The first step is to design the ripple-rejection voltage-feedback ($V_{dc,i}$, where i = 1, 2, …., m) controller for each input port, with neglecting the average ripple-capacitor voltage (V_{opd}) controller. The ripple rejection controller includes two sub-controllers: (1) PI controller, and (2) feed-forward controller. First, by neglecting the feed-forward part, the PI controller is designed for each input port, and then the feed-forward controller is designed. The main issue of the design procedure is that since the DC-component of the DC-link is controlled by the main inverter controller, the ripple rejection control loop should exclude the DC component in the feedback information while it has a high loop-gain at the ripple frequency, 120 Hz, and other side-band harmonic components. After the

ripple rejection controller design, the second step is to design the ripple-capacitor average-voltage controller along with the closed control-loop of the input-port ripple rejection controller. The key point in the design is that it must allow the ripple frequency, 120 Hz, and other harmonic components of the voltage to swing freely around the average voltage value, in order to fully absorb the ripple components from the DC-link. Hence, it is preferable to design the average voltage controller bandwidth to be far lower than the ripple frequency.

A more detailed design procedure of the proposed power-decoupling control scheme is described as follows.

First, the PI controller for the ripple rejection controller is tentatively designed without the outer ripple-capacitor voltage loop. The loop-gain of the PI controller for the ripple rejection controller, $T_{vdc-pi}(s)$, is derived from the figure as in eq. (25):

$$T_{vdc-pi}(s) = HPF(s)PI_{vdc-i}(s)G_{vdc-i}(s) \qquad (25)$$

Where,

$$PI_{vdc-i}(s) = k_{pdf-i} + \frac{k_{idf-i}}{s}; \; HPF(s) = \frac{s^2}{s^2 + 2\xi\omega_c s + \omega_c^2}$$

After designing the PI controller for each ripple rejection controller, the other controller in feed-forward is designed, and it completes the ripple rejection controller. The loop gain of ripple rejection controller with the feed-forward controller gain, K_{ff-i}, is obtained in eq. (26):

$$T_{vdc-ff} = \frac{HPF(s)PI_{vdc-i}G_{vdc-i}(s)}{1 - K_{ff-i}HPF(s)(mG_{vopd}(s) - G_{vdc-i}(s))}$$

$$(26)$$

MATLAB software has been used to design the control loops, and draw the Bode plots for $T_{vdc-pi}(s)$ and $T_{vdc-ff}(s)$. The parameters of the ripple rejection controller are, $k_{pdf-1} = -2.2$, $k_{idf-1} = -1.35$, and $K_{ff-1} = 0.1$. Figure 11 shows the Bode plot of the PI controller loop gain, $T_{vdc-pi}(s)$. This shows that the DC component is out of the control of the controller design, as it has a zero at DC (90 degree in the phase). Whereas, the loop gain of the ripple rejection controller, $T_{vdc-pi}(s)$, is 43.9 dB at 120 Hz, and maintains a high level around the harmonic area, which is sufficient to suppress the ripple frequency component in the inverter DC-link. Since the three input ports of the symmetric H-bridge cascaded inverter are considered that have a similar voltage-ripple profile, the same ripple rejection controller design is applied to the other two input ports.

Secondly, the average voltage controller for the ripple capacitor at the DHB secondary is designed using the block diagram in Fig. 10. The average voltage loop gain including the closed-loop ripple rejection controller is derived as eq. (27)

Figure 12 shows the Bode plot of a design result for $T_{vopd}(s)$. The coefficients are $k_{pvopd} = 0.24$ and $k_{ivopd} = 1$. The loop gain of the average voltage controller, $T_{vopd}(s)$, has a bandwidth of 8 Hz. The Bode plot shows that the controller has an infinite DC gain, and
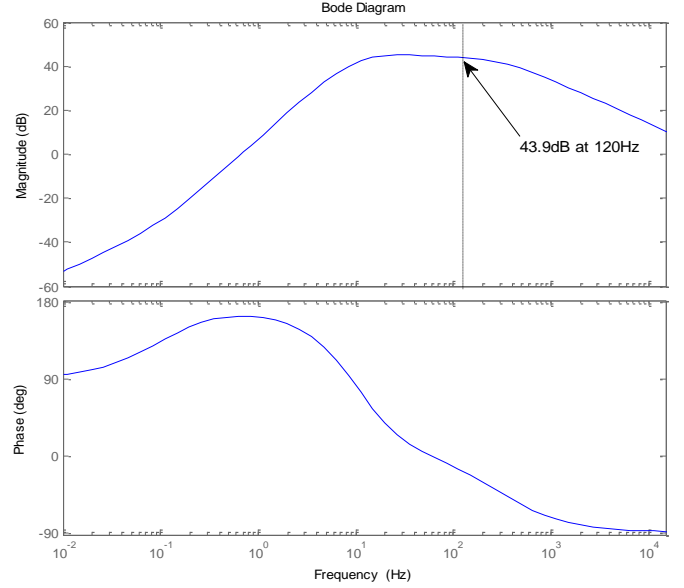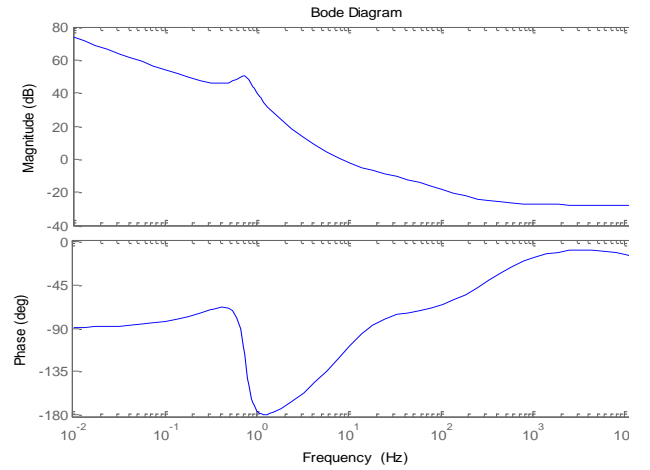

Fig. 11: Bode plot for $T_{vdc-pi}(s)$.

Fig. 12: Bode plot for $T_{vopd}(s)$ with $k_{pvopd} = 0.24$ and $k_{ivopd} = 1$

average voltage controller, $T_{vopd}(s)$, has a bandwidth of 8 Hz. The Bode plot shows that the controller has an infinite DC gain, and also that the ripple frequency components are located out of the control bandwidth.

After the voltage controller design, the design comes back to the DC-link ripple controller for accurate analysis. The expression of $T_{vdc}(s)$ including the outer loop is obtained as in eq. (28):

$$T_{vopd}(s)\Big|_{v_{DC-i_{ref}}(s)=0} = \frac{mPI_{vopd}(s)G_{vopd}(s)}{1 + HPF(s)PI_{vdc-i}(s)G_{vdc-i}(s) + HPF(s)K_{ff-i}G_{vdc-i}(s) - mHPF(s)K_{ff-i}G_{vopd}(s)}$$

$$(27)$$

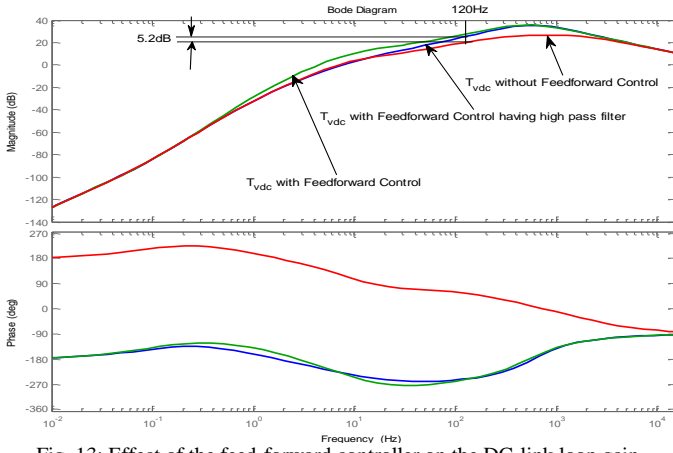$$\text{where, } PI_{vopd}(s) = k_{pvopd} + \frac{k_{ivopd}}{s}$$

Fig. 13: Effect of the feed-forward controller on the DC-link loop gain, including the average voltage controller with and without high pass filter in feed-forward.
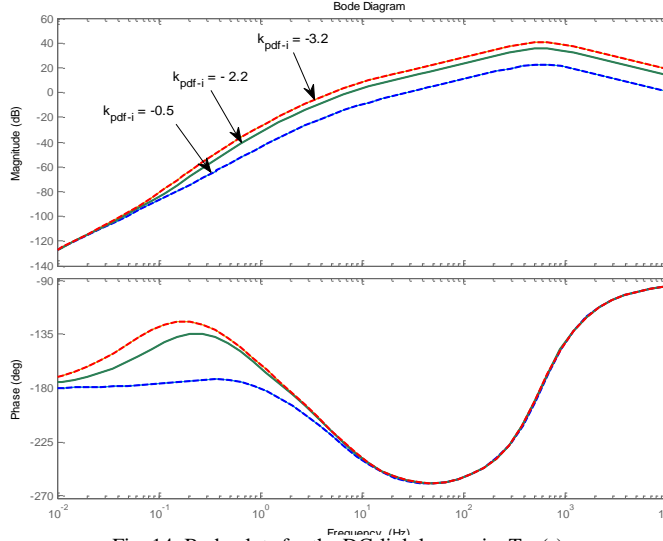

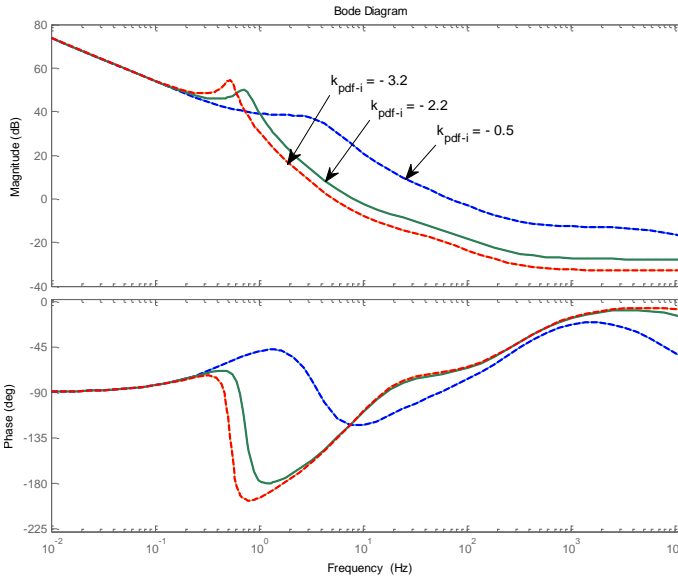Fig. 14: Bode plots for the DC-link loop gain, $T_{vdc}(s)$.

Fig. 15: Bode plots for the average voltage loop gain, $T_{vopd}(s)$.

$$T_{vdc}(s) = \frac{HPF(s)PI_{vdc-i}(s)G_{vdc-i}(s)}{1 + mPI_{vopd}(s)G_{vopd}(s) - HPF(s)K_{ff-i}\left(mG_{vopd} - G_{vdc-i}\right)}$$

(28)

Figure 13 shows the dynamics effect of the feed-forward control on the DC-link voltage loop gain. By the feed-forward control in the ripple rejection controller, the DC-link loop gain increases by 5.2 dB at 120 Hz, which means the double-frequency voltage ripple decreases by a factor of 1.8. Finally, Figs. 14 and 15 show Bode plots of the DC-link loop gain, $T_{vdc}(s)$, and of the average voltage control loop, $T_{vopd}(s)$, with feed-forward control.

Figures 14 and 15 show that the loop gains, $T_{vdc}(s)$ and $T_{vopd}(s)$, are plotted with k_{pdf-i} = -0.5, -2.2, and -3.2 in the PI controller. The DC-link loop gain, $T_{vdc}(s)$, is increased from 12.2 to 25.1 dB at 120 Hz, as k_{pdf-i} decreases from -0.5 to -2.2. The Bode plots clearly show that as k_{pdf-i} decreases, the loop gain, $T_{vdc}(s)$ increases, and therefore, the double frequency ripple decreases. Whereas, when k_{pdf} decreases, the bandwidth and phase margin of the average voltage controller $T_{vopd}(s)$ also decrease. With k_{pdf-i} = -3.2, the crossover frequency is below 5 Hz, and the phase margin is less than 45°, which is not preferable. Therefore, there is a trade-off on decreasing the value of k_{pdf-i}. In actual test with this value of k_{pdf-i}, the power-decoupling controller design malfunctions. Therefore, k_{pdf-i} = -2.2 is preferred under the trade-offs. From the discussion, it can be known that as k_{pdf-i} decreases, the DC-link double frequency ripple decreases, whereas the phase margin of the average voltage controller decreases. Therefore, the controller parameters are determined by the trade-offs between the DC-link power-decoupling performance, and the stability of the outer voltage loop.

V. HARDWARE VERIFICATION

The proposed power-decoupling multi-port DHB circuit with a single ripple-rejection capacitor for a symmetric cascaded H-bridge multi-level inverter is validated by means of simulation and experimental results with a 1.2-kW hardware prototype. The simulation is accomplished by PSIM. The power-decoupling control scheme is implemented with a DSC TMS320F28335 platform. The experimental verification is performed by the hardware prototype shown in Fig. 16. Table III summarizes the key parameters for simulation and the experimental results. The verification of the multiport transformer design is performed by the multi-port DHB converter efficiency. In this section, the verification of the proposed power-decoupling control scheme for the multi-level inverter is conducted by simulation and experimental results using a multi-port DHB converter, followed by hardware measurement of the power conversion efficiency.
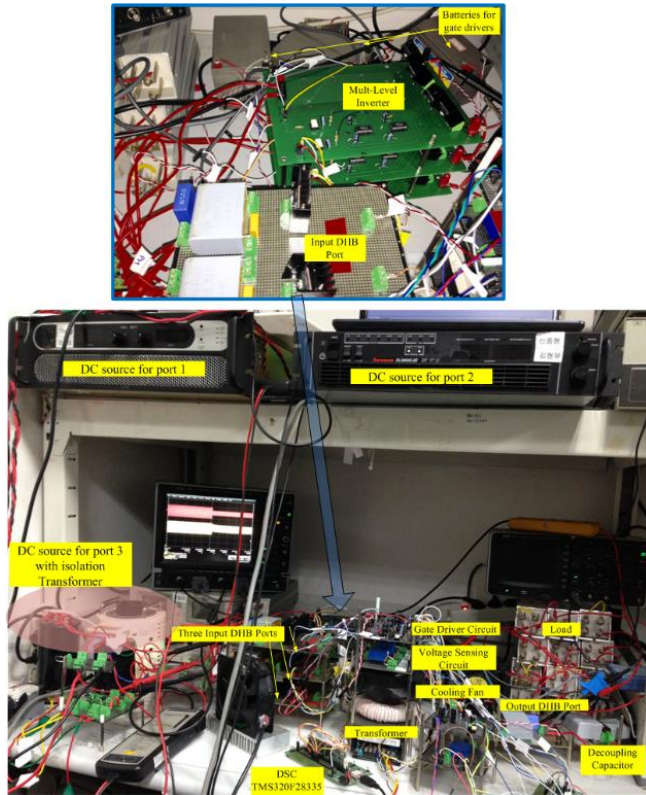
Fig. 16: Experimental step-up for testing the power-decoupling of the multilevel inverter

TABLE III.
KEY PARAMETERS FOR THE HARDWARE PROTOTYPE

Circuit Parameters	Quantity	Value
P	Output Power	1.2 kW
V_o	Multilevel inverter Output Voltage	346 Vrms with 60 Hz
f_s	Switching Frequency	30 kHz for multi-port DHB 4 kHz for CHB
V_{dc-i}, i =1,2,3	DC- Link Voltage	200 V
V_{opd}	Average voltage across Power-decoupling Capacitor	200 V
	Swing of Voltage	160 V
L_{pi} i=1,2,3	Leakage Inductance of each port	32 µH, 35 µH, 37 µH
L	Inductor on secondary side of the transformer	13 µH
$C_{pi}/2$ i=1,2,3	Individual DC link Capacitance	25 µF
Transformer's windings turns	Number of turns in input ports windings	50
	Number of turns in output winding	56
r_{DSon} *for* S_{i1}/S_{i2}	*Resistance of input ports' switches for* S_{i1}/S_{i2} *(IRFP4868PbF)*	25.5 mΩ
r_{DSon} *for* S_1/S_2	*Resistance of power decoupling port's switches(UJC1206K)*	42 mΩ
r_t	Transformer windings' resistance	0.33 Ω

Figure 17 shows the steady-state waveforms of the simulation and hardware experiment, at DC-link voltage, multi-level PWM output voltage, and the voltage across the power-decoupling capacitor. From the simulation and experimental waveforms, it is clear that the DC-Link voltage double frequency is reduced to within 10% of the DC-link average voltage, 200 V, with film capacitors of about 100 µF decoupling capacitance for all the three cells of the symmetric multilevel inverter, instead of mF-level electrolytic ones. The experimental and numerical waveforms show that the double-frequency ripple power in every H-bridge cell is well absorbed by the power-decoupling DHB converter using a large swing of the ripple capacitor voltage.
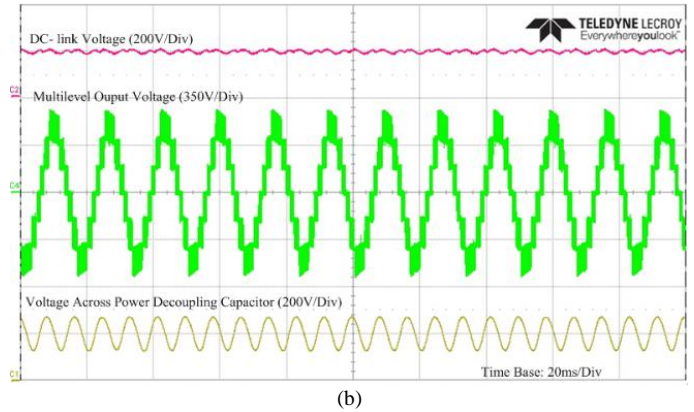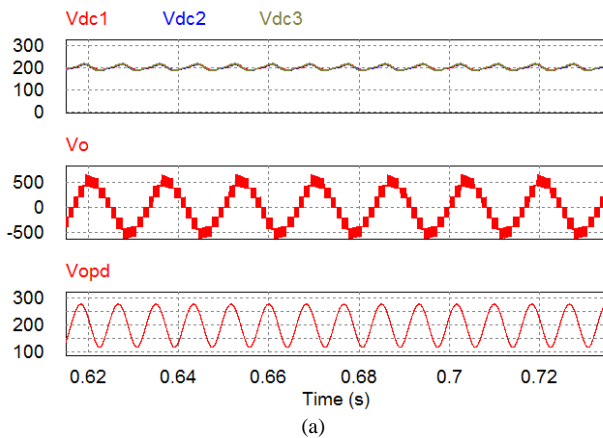

(a)

(b)

Fig. 17 (a): Key waveforms of numerical analysis: DC-Link voltages of all the three cells of multilevel inverter (V_{dc1}, V_{dc2}, V_{dc3}), voltage across the power-decoupling capacitor (V_{opd}), and output voltage of the multilevel inverter (V_O); and (b) Experimental key waveforms: DC-Link voltage, output voltage of the multilevel inverter, and Voltage across the power-decoupling Capacitor. Both results agree well with each other.
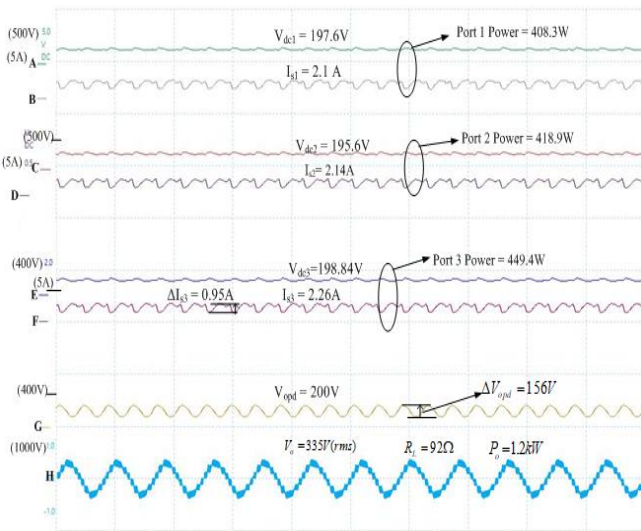
Fig. 18: Experimental key waveforms: DC-Link 1 voltage,V_{dc1} , DC source -1 current, I_{s1}, DC-Link 2 voltage,V_{dc2}, DC source -2 current, I_{s2}, DC-Link 3 voltage,V_{dc3} , DC source -3 current, I_{s3}, voltage across power decoupling capacitor, and output voltage of Multilevel inverter.

Due to the proposed power-decoupling control scheme, it becomes possible to compensate the double frequency voltage ripple of all the three cells of the multilevel inverter by one power-decoupling capacitor, which reduces the size of the power-decoupling circuit. The average voltage across the power-decoupling capacitor is designed to be regulated at 200 V, and it is shown that it is well maintained at that voltage in simulation, as well as in the experiment. The equation for the power-decoupling capacitance eq. (2) [21] shows the voltage swing across the power-decoupling capacitor to be 159 V, and the actual one in the experimental result is 156V.

Both waveforms of the simulation and hardware almost agree with each other, and the small difference may come from the power losses, due to the non-ideal device characteristics, as well as the circuit layout parasitic components. Fig. 18 shows the real time waveforms captured by 8-channel oscilloscope. Figure 18
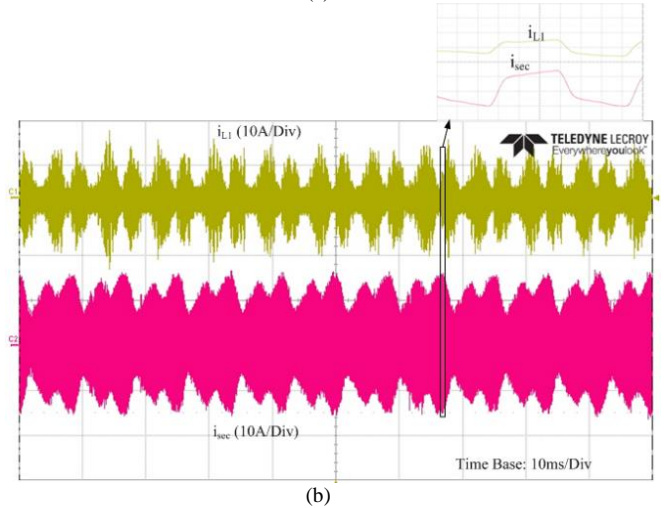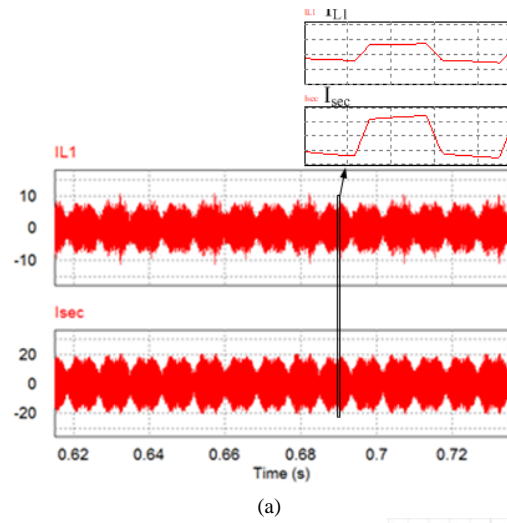
Fig. 19. Key waveforms (a) Numerical analysis: Transformer input port 1, I_{L1} current and output port current I_{sec}, and (b) Hardware experiment: Transformer input port 1 current and the output port current
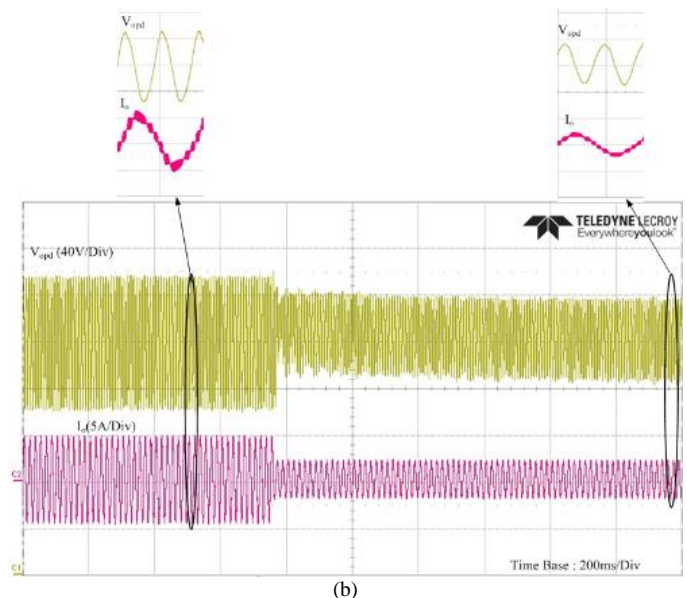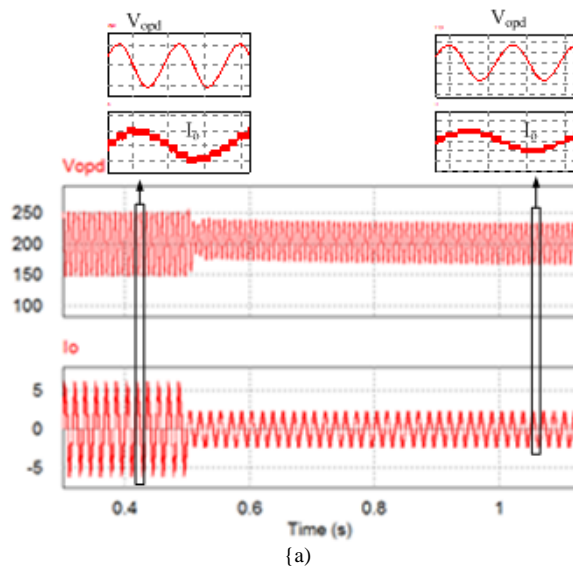

Fig. 20. Transient waveforms (a) Simulation under a load step of the proposed power-decoupling control scheme, and (b) Hardware experiment under a load step of the proposed power-decoupling control scheme

shows the waveforms of all the three DC-link voltages of the multilevel inverter, V_{dc1}, V_{dc2} and V_{dc3}, all dc-sources current, I_{s1}, I_{s2} and I_{s3}, voltage across power decoupling capacitor and the multilevel PWM output voltage, Vo. the dc-sources' current average current is 2.17 A. The DC-link voltage waveforms of the three DC-link voltages also have power-decoupled waveforms, and their average is identically located at 200 V.

Figure 19 shows the simulation and experimental waveforms of the multi-port transformer currents, input port 1, IL1, and output port, Isec. The currents through the other two input ports are also very similar to the figure. The figure shows that both the simulation and experimental waveforms in steady state response are in accordance. A ripple frequency envelop means the ripple-rejection circuit well delivers the ripple power into the secondary-side ripple capacitor. Figure 20 shows a load-transient response of the proposed power-decoupling control scheme. The load is step-changed from 1 kW to 500 W. The dynamic response of the proposed power-decoupling control scheme from the simulation and experimental results validates the stability and accuracy of the transient analysis and design guidelines for the proposed power-decoupling control scheme with multilevel inverters.

The efficiency plots for the multilevel inverter with power decoupling circuit and with electrolytic capacitors is shown in fig. 21. The efficiency of the multilevel inverter with power decoupling circuit at rated power, 1.2kW, is 95.67 % and with electrolytic capacitor is 97.1%. Therefore, the decrease in efficiency is 1.43%. The decrease in efficiency of the multilevel inverter is nominal with active decoupling circuit. The efficiency of multiport dual half-bridge converter as a power decoupling circuit by neglecting the multilevel inverter is also shown in Fig. 21. The efficiency of the multiport dual half-bridge converter as a power decoupling circuit on neglecting multilevel inverter at rated power is 97.5%. This high value comes from the proposed design procedure, considering the complex loss breakdown of the multi-port DHB transformer related to the parameters, such as phase-shift, switching frequency, number of turns in the winding, and leakage inductances.

VI. CONCLUSION

A generalized power-decoupling control scheme without current sensors is presented for a symmetric cascaded H-bridge multi-level inverter by using a multi-input port/single output DHB converter as a power-decoupling circuit. Film capacitors are implemented instead of the electrolytic ones, to improve the lifetime and reliability. With the proposed power-decoupling method, the double frequency ripple power at all the DC-links can be directed to a common magnetic circuit, and the total ripple power is able to link to a single power-decoupling capacitor. Hence, a multi-level inverter power-decoupling is achieved by one power-decoupling capacitor. This gives an optimized solution in terms of cost and size. In the multi-port dual half bridge converter, the multi-port transformer is one of the major concerns with regard to the efficiency of the converter. This paper proposed a design methodology for designing the multiport transformer. To design the transformer, expressions of the RMS currents through the transformer are obtained. The transformer's currents are dependent on the switching frequency, leakage inductance, phase-shift, and the output voltage. The design methodology for the transformer is significant, due to the non-linear and complex behavior of the transformer currents. With the proposed design methodology, the efficiency of the hardware prototype is 95.67% at 1.2 kW. A generalized power-decoupling control for the multi-level inverter is proposed in this paper. The proposed control scheme is of the current-sensorless type, and the fast voltage dynamics based on the sensorless control gives the advantage of using a universal "zero" reference to eliminate the double frequency ripple voltage. Therefore, the proposed control scheme is independent of the multi-level inverter topology, architecture, or control strategies. The bandwidth of the power-decoupling controller can be increased without any inner feedback loop, due to the small capacitance and single-pole behavior of the multi-input/single output bidirectional DHB converter. The analysis and design guidelines of the proposed power-decoupling control scheme are presented. The control design shows the effect of the feedforward controller on the elimination of the DC-link ripple. The proposed power-decoupling method is able to reduce the voltage ripple at all the DC-links in the multi-level inverter to 10% at the DC-links with an equivalent film capacitor of about 100 μF for 1.2 kW. The results of experiments under the steady state and transient operation are obtained through 1.2-kW simulation and hardware tests. The proposed power-decoupling control method for the multi-level inverter by a multi-port DHB converter is verified, and shows a promising ability to provide universal power-decoupling for any type of multi-level inverter.
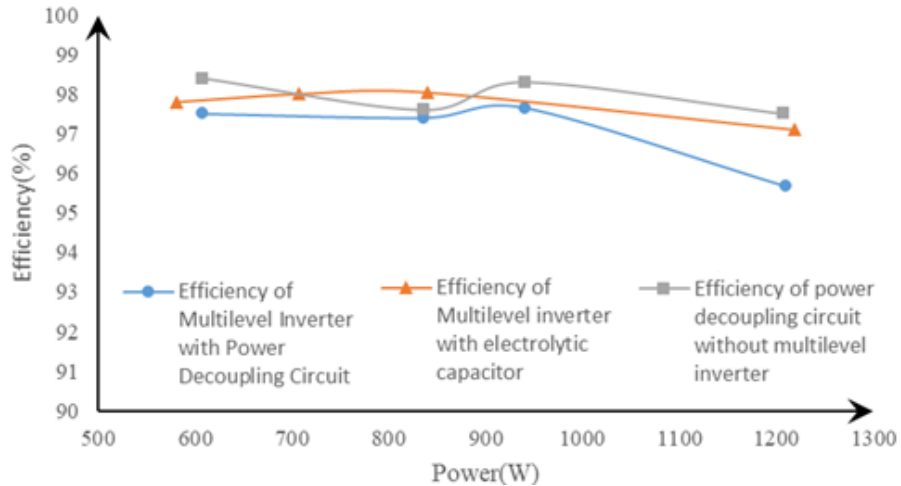

Fig. 21. Hardware measurement efficiency plot

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